個人

Greatest common divisor:

- It's better to draw a diagram of the top module.

- The explanation for the design could be more detailed.

Take Away Part:

- I am glad that you mentioned about making the circuit efficient and removing redundant parts.

- Although you might not have sufficient time for this lab, you can keep that concept in mind. They will be useful in the future.

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Sliding window sequence detector: FAIL

Traffic light controller: PASS

Greatest common divisor: PASS

Booth multiplier: PASS

組別

FPGA:

- Design 的部分可以解釋詳細一點

-No state transition diagram

- Please explain how you test your design.

FPGA2:

-要說明如何測試design

-可以再多解釋你的design

Take Away Part:

- Glad to know that you have learned how to use peripheral devices and the interaction of them with FPGA.

- Great to hear that you can apply the concept of finite state machines to this FPGA questions.

- You can share more about what you have learned form this FPGA assignment to make it more comprehensive.